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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,016	01/02/2002	Robert C. Glenn	42390P12278	7520

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,016	GLENN ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,17,25 and 28* is/are rejected.

7)☒ Claim(s) *3-6,8-16,18-24,26,27,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "*phase interpolator coupled with said phase controller to change a phase of the recovered clock ... weighted in accordance with the interrelated control signals*" must be shown "*in figure 1*" or the feature(s) canceled from the claim(s). No new matter should be entered. *Examiner's comments*: it appears in figure 1 that the interrelated control signals is generated by the phase interpolator 150.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 7, 17, 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchwald et al. U.S Patent 6,509,733 B2.

Regarding claim 1, referring to figure 3, in column 9 lines 3-67, Buchwald et al. teaches a timing recovery module 202 comprising:

- a phase controller 302 including data path 308, a phase path 310, a phase detector 312 coupled to the data and phase paths, and a phase error processor 314 coupled to the phase detector; see column 9, lines 4-67. The phase controller 302 produces a plurality of digital control signals 340, which correspond to the claimed interrelated control signals, based on a comparison of data signal 346 and a phase signal 348. The phase signal 348 is the recovered clock as claim because the phase signal 348 includes a series of phase samples also indicative of serial data signal 104; see column 9, lines 45-60;

- a phase interpolator 306 coupled with the phase controller 302 producing timing/sampling signal 208 and a second timing/sampling signal 344 offset in phase from sampling signal 208, based on reference signal set 206 and a plurality of digital control signals 340 applied to the phase interpolator.

Buchwald et al. does not expressly teach the claimed limitations "*a phase interpolator to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from more than one phase are weighted in accordance with the interrelated control signals*". In column 9, lines 20-27, see also figure 3, Buchwald et al. teaches that signal set generator 334 generates a set of reference signals 206, all having the same frequency but different predetermined phases. As recited above, the phase signal 348 is the recovered clock as claim because the phase signal 348 includes a series of phase samples. In light of the foregoing discussion, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the phase interpolator 306 changes a phase of the second timing/sampling signal 344 based on the set of reference signals 206 having the same frequency but different predetermined phases. Furthermore, the phase interpolator 306 also receives a plurality of digital control signals 340 generated by the

controller 302. As result of that, the amplitude contributions from more than one phase are weighted in accordance with the plurality of digital control signals 340.

Regarding claim 2, Buchwald et al. invention differs from the instant application in that the phase detector 312 is part of the phase controller 302. Despite of the slight difference, one of ordinary skill in the art would have recognized that the claimed limitations are within the scope of Buchwald et al. teachings. Furthermore, phase detector 312 detects a phase error between data sampling 208 and serial data signal 104 based on the data samples in data signal 346 and the phase samples in phase signal 348, which determines the sample rate of phase detector 312; see column 9, lines 58-67. As recited above, the phase signal 348 is equivalent to the claimed recovered clock signal.

Regarding claim 7, referring to figure 3, in column 9, lines 19-27, signal set generator 334 generates the set of reference signals 206 based on reference signal 336. The reference signal 336, corresponding to the claimed reference clock, is coupled to the phase interpolator 306 to generate a reference signal 206 having different predetermined phases.

Regarding claim 17, claim 17 is rejected on the same ground as for claim 2 because of similar scope. Claim 2 claims all elements that can perform all steps of claim 17.

Regarding claim 25, referring to figure 3, in column 9 lines 3-67, Buchwald et al. teaches a timing recovery module 202 comprising:

- Figure 1 shows a communication system 100 including a transmitter 100 and a receiver 102. The receiver 102 includes a front-end receiver to amplify the data as appreciated by one of ordinary skill in the art.
- a phase controller 302 including data path 308, a phase path 310, a phase detector 312 coupled to the data and phase paths, and a phase error processor 314 coupled to the phase detector; see column 9, lines 4-67. The phase controller 302 produces a plurality of digital control signals 340, which correspond to the claimed interrelated control signals, based on a comparison of data signal 346 and a phase signal 348. The phase signal 348 is the recovered clock as claim because the phase signal 348 includes a series of phase samples also indicative of serial data signal 104; see column 9, lines 45-60. Buchwald et al. invention differs from the claimed invention in that Buchwald et al. teaches that the phase controller 302 includes the phase detector 312, corresponding to the claimed phase-frequency detector, the phase error processor 314, phase control signal rotator 304. Nevertheless, phase control signal rotator 304 is coupled to the phase error processor 314 to generate

interrelated control signals based upon the phase error signal from the phase error processor 314. In light of that, one of ordinary skill in the art would have recognized that the phase control signal rotator 304 performs equivalent function of the claimed phase controller and the phase error processor 314 performs equivalent function of the claimed phase update logic circuitry.

- a phase interpolator 306 coupled with the phase controller 302 producing timing/sampling signal 208 and a second timing/sampling signal 344 offset in phase from sampling signal 208, based on reference signal set 206 and a plurality of digital control signals 340 applied to the phase interpolator.

Buchwald et al. does not expressly teach the claimed limitations "*a phase interpolator to change a phase of the recovered clock signal with an analog transition based upon a combination of amplitude contributions from more than one phase of a reference clock signal, wherein the amplitude contributions from more than one phase are weighted in accordance with the interrelated control signals*". In column 9, lines 20-27, see also figure 3, Buchwald et al. teaches that signal set generator 334 generates a set of reference signals 206, all having the same frequency but different predetermined phases. As recited above, the phase signal 348 is the recovered clock as claim because the phase signal 348 includes a series of phase samples. In light of the foregoing

discussion, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the phase interpolator 306 changes a phase of the second timing/sampling signal 344 based on the set of reference signals 206 having the same frequency but different predetermined phases. Furthermore, the phase interpolator 306 also receives a plurality of digital control signals 340 generated by the controller 302. As result of that, the amplitude contributions from more than one phase are weighted in accordance with the plurality of digital control signals 340.

Regarding claim 28, claim 28 is rejected on the same ground as for claim 17 because similar scope. Furthermore, one of ordinary skill in the art would have recognized that the method of claim 17 can be implemented as computer instructions storing on computer hard drive, the computer instructions is executed to cause the computer performing the claimed steps.

Allowable Subject Matter

3. Claims 3-6, 8-16, 18-24, 26-27 and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Anderson U.S Patent 6,122,336 discloses "Digital Clock Recovery Circuit With Phase Interpolation".

Donnelly et al. U.S Patent 6,122,336 discloses "Delay-Locked Loop Circuitry For Clock Delay Adjustment".

Lee et al. U.S 2002/0085656 A1 discloses "Data Recovery Using Data Eye Tracking".

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 03/18/2005
Examiner KHANH TRAN